PRELIMINARY

Some of contents are subject to change without notice.

DESCRIPTION

M2S28D20ATP is a 4-bank x 8388608-word x 4-bit,
M2S28D30ATP is a 4-bank x 4194304-word x 8-bit,
M2S28D40ATP is a 4-bank x 2097152-word x 16-bit,
double data rate synchronous DRAM, with SSTL_2 interface. All control and address signals are referenced to the rising edge of CLK. Input data is registered on both edges of data strobe, and output data and data strobe are referenced on both edges of CLK. The M2S28D20/30/40ATP achieves very high speed data rate up to 133MHz, and are suitable for main memory in computer systems.

FEATURES

- Vdd=Vddq=2.5V±0.2V
- Double data rate architecture;
  two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data
- Differential clock inputs (CLK and /CLK)
- DLL aligns DQ and DQS transitions
  with CLK transitions edges of DQS
- Commands entered on each positive CLK edge;
- data and data mask referenced to both edges of DQS
- 4 bank operation controlled by BA0, BA1 (Bank Address)
- /CAS latency- 2.0/2.5 (programmable)
- Burst length- 2/4/8 (programmable)
- Burst type- sequential / interleave (programmable)
- Auto precharge / All bank precharge controlled by A10
- 4096 refresh cycles /64ms (4 banks concurrent refresh)
- Auto refresh and Self refresh
- Row address A0-11 / Column address A0-9,11(x4)/ A0-9(x8)/ A0-8(x16)
- SSTL_2 Interface
- 400-mil, 66-pin Thin Small Outline Package (TSOP II)
- FET switch control(/QFC) for x4/ x8
- JEDEC standard

PIN CONFIGURATION(TOP VIEW)

x4	x8	x16	Pin	Pin	x16	x8	x4
VDD	VDD	VDD	1	66	VSS	VSS	VSS
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	NC	NC	NC
VDD	VDD	VDD	18	49	VREF	VREF	VREF
NU,/QFC	NU,/QFC	NC	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
/WE	/WE	/WE	21	46	/CLK	/CLK	/CLK
/CAS	/CAS	/CAS	22	45	CLK	CLK	CLK
/RAS	/RAS	/RAS	23	44	CKE	CKE	CKE
/CS	/CS	/CS	24	43	NC	NC	NC
NC	NC	NC	25	42	NC	NC	NC
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

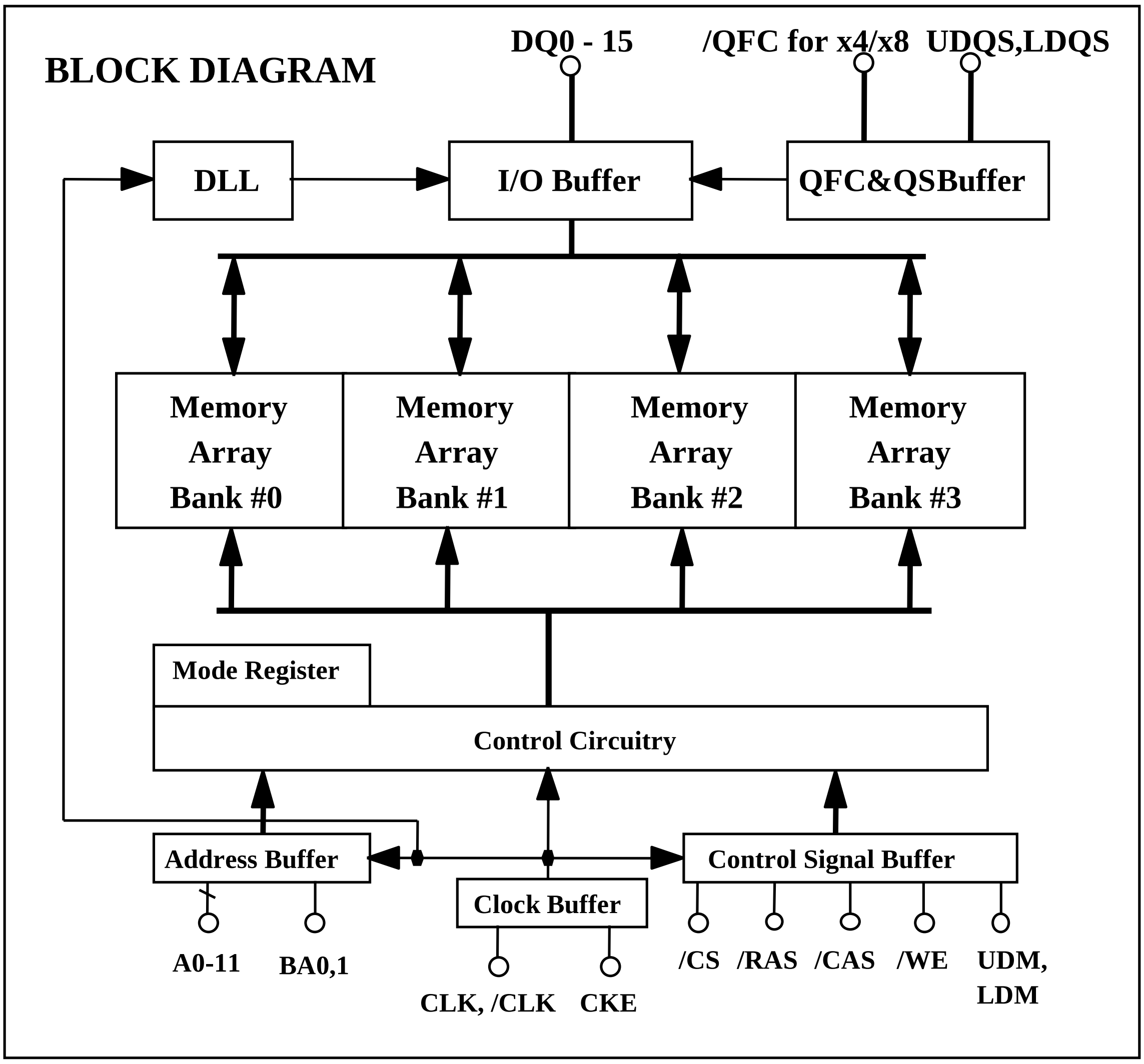
66pin TSOP(II)

400mil width x 875mil length

0.65mm Lead Pitch

ROW
A0-11
Column
A0-9,11(x4)
A0-9 (x8)
A0-8 (x16)

CLK,/CLK	**: Master Clock**	**A0-11**	**: Address Input**
CKE	**: Clock Enable**	**BA0,1**	**: Bank Address Input**
/CS	**: Chip Select**	**Vdd**	**: Power Supply**
/RAS	**: Row Address Strobe**	**VddQ**	**: Power Supply for Output**
/CAS	**: Column Address Strobe**	**Vss**	**: Ground**
/WE	**: Write Enable**	**VssQ**	**: Ground for Output**
DQ0-7	**: Data I/O**		
DQS	**: Data Strobe**		
DM	**: Write Mask**		
/QFC	**: FET Switch Control for x4/x8**		
Vref	**: Reference Voltage**		



Type Designation Code

This rule is applied to only Synchronous DRAM family.

M 2 S 28 D 3 0 A TP -75

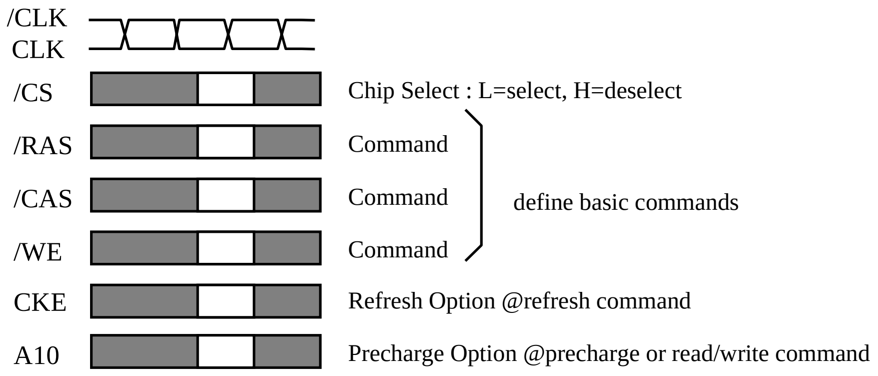
- -75: Speed Grade 10: 125MHz@CL=2.5,100MHz@CL=2.0; 75: 133MHz@CL=2.5,100MHz@CL=2.0
- TP: Package Type TP: TSOP(II)
- A: Process Generation
- 0: Function Reserved for Future Use
- 3: Organization 2^n 2: x4, 3: x8, 4: x16
- D: **DDR Synchronous DRAM**
- 28: Density 28: 128M bits
- S: Interface V:LVTTL, S:SSTL_3, _2
- 2: Memory Style (DRAM)
- M: Mitsubishi Main Designation

PIN FUNCTION

SYMBOL	TYPE	DESCRIPTION
CLK, /CLK	Input	Clock: CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-11	Input	A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-9,11(x4), A0-9(x8) and A0-8(x16). A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
DQ0-15(x16), DQ0-7(x8), DQ0-3(x4),	Input / Output	Data Input/Output: Data bus
DQS	Input / Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS correspond to the data on DQ8-DQ15
/QFC	Output	FET Control: Optional. Output during every Read and Write access. Can be used to control isolation switches on modules. Open drain output.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.
Vref	Input	SSTL_2 reference voltage.

BASIC FUNCTIONS

The M2S28D20/30/40ATP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS ,CKE and A10 are used as chip select, refresh option, and precharge option, respectively. To know the detailed definition of commands, please see the command truth table.



Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, **READA)**

Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA)**

Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read /write operation. When A10 =H at this command, all banks are deactivated (precharge all, **PREA**).

Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	BA0,1	A10 /AP	A0-9, 11	note
Deselect	DESEL	H	X	H	X	X	X	X	X	X	
No Operation	NOP	H	X	L	H	H	H	X	X	X	
Row Address Entry & Bank Activate	ACT	H	H	L	L	H	H	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	V	L	X	
Precharge All Banks	PREA	H	H	L	L	H	L	X	H	X	
Column Address Entry & Write	WRITE	H	H	L	H	L	L	V	L	V	
Column Address Entry & Write with Auto-Precharge	WRITEA	H	H	L	H	L	L	V	H	V	
Column Address Entry & Read	READ	H	H	L	H	L	H	V	L	V	
Column Address Entry & Read with Auto-Precharge	READA	H	H	L	H	L	H	V	H	V	
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	
		L	H	L	H	H	H	X	X	X	
Burst Terminate	TERM	H	H	L	H	H	L	X	X	X	1
Mode Register Set	MRS	H	H	L	L	L	L	L	L	V	2

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0=1 , BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A11 provide the op-code to be written to the selected Mode Register.

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
IDLE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA	
	L	L	H	L	BA, A10	PRE / PREA	NOP	4
	L	L	L	H	X	REFA	Auto-Refresh	5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set	5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	NOP	
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ(Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	Terminate Burst	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
WRITE(Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge	3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ with Auto-Precharge	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE with Auto-Precharge	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
PRE-CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)	
	L	H	H	H	X	NOP	NOP (Idle after tRP)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	NOP (Idle after tRP)	4
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)	
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
REFRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)	
	L	H	H	H	X	NOP	NOP (Idle after tRC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Row Active after tRSC)	
	L	H	H	H	X	NOP	NOP (Row Active after tRSC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

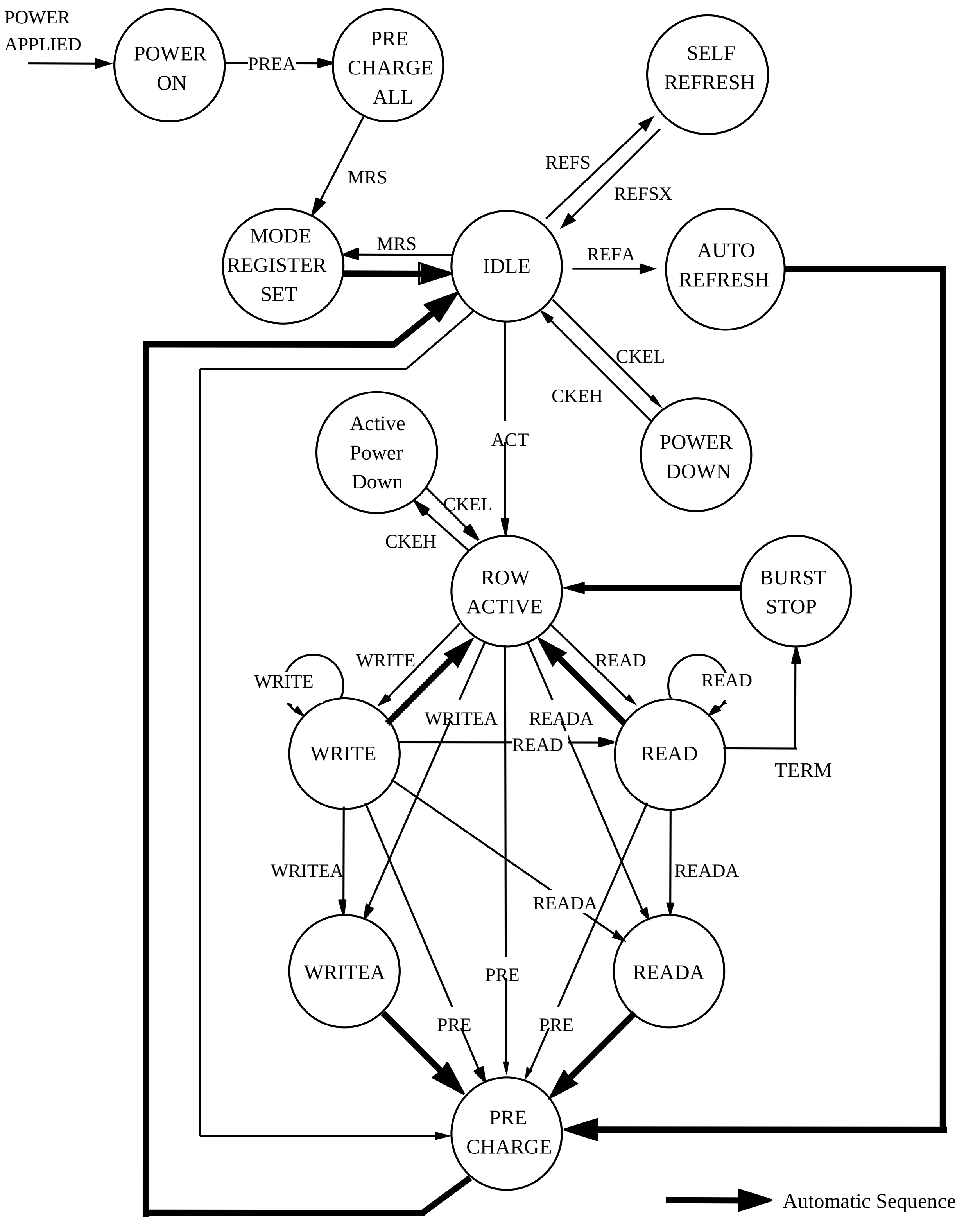
FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Address	Action	Notes
SELF-REFRESHING	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)	1
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	L	X	X	ILLEGAL	1
	L	H	L	L	X	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)	1
POWER DOWN	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power Down to Idle	
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)	
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function Truth Table	2
	H	L	L	L	L	H	X	Enter Self-Refresh	2
	H	L	H	X	X	X	X	Enter Power Down	2
	H	L	L	H	H	H	X	Enter Power Down	2
	H	L	L	H	H	L	X	ILLEGAL	2
	H	L	L	H	L	X	X	ILLEGAL	2
	H	L	L	L	X	X	X	ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Current State =Power Down	2
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle	3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle	3
	L	L	X	X	X	X	X	Maintain CLK Suspend	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. CKE Low to High transition will re-enable CLK and other inputs asynchronously.
   A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

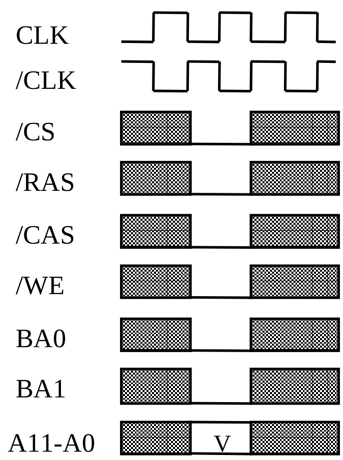
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or multifunctioning.

1. Apply VDD before or the same time as VDDQ
2. Apply VDDQ before or at the same time as VTT & Vref
3. Maintain stable condition for 200us after stable power and CLK, apply NOP or DSEL
4. Issue precharge command for all banks of the device
5. Issue EMRS
6. Issue MRS for the Mode Register and to reset the DLL
7. Issue 2 or more Auto Refresh commands
8. Maintain stable condition for 200 cycle

After these sequence, the DDR SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After tRSC from a MRS command, the DDR SDRAM is ready for new command.



BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	DR	0	LTMODE			BT	BL		

	CL	/CAS Latency
Latency Mode	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	R
	1 0 0	R
	1 0 1	R
	1 1 0	2.5
	1 1 1	R

	BL	BT=0	BT=1
Burst Length	0 0 0	R	R
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	R	R

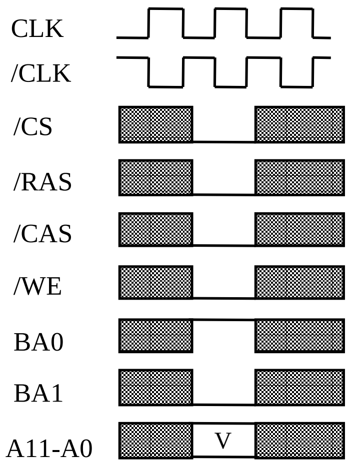
Burst Type	0	Sequential
	1	Interleaved

DLL Reset	0	NO
	1	YES

R: Reserved for Future Use

EXTENDED MODE REGISTER

DLL disable / enable mode can be programmed by setting the extended mode register (EMRS). The extended mode register stores these data until the next EMRS command, which may be issued when all banks are in idle state. After tRSC from a EMRS command, the DDR SDRAM is ready for new command.

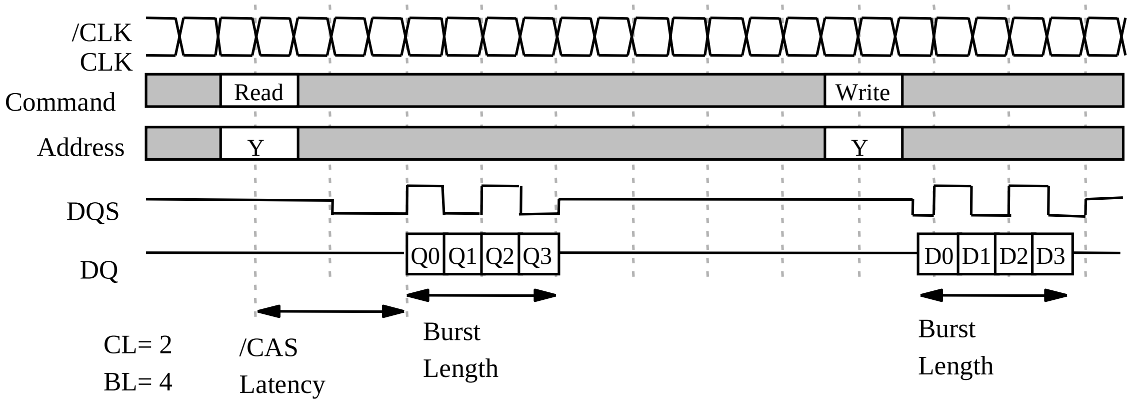


BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	0	0	QFC	DS	DD

DLL Disable		
	0	DLL Enable
	1	DLL Disable

Drive Strength		
	0	Normal
	1	Weak

QFC		
	0	Disable
	1	Enable



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 3.7	V
VddQ	Supply Voltage for Output	with respect to VssQ	-0.5 ~ 3.7	V
VI	Input Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
VO	Output Voltage	with respect to VssQ	-0.5 ~ VddQ+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25 ^{o}C	1000	mW
Topr	Operating Temperature		0 ~ 70	^{o}C
Tstg	Storage Temperature		-65 ~ 150	^{o}C

DC OPERATING CONDITIONS

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Notes
		Min.	Typ.	Max.		
Vdd	Supply Voltage	2.3	2.5	2.7	V	
VddQ	Supply Voltage for Output	2.3	2.5	2.7	V	
Vref	Input Reference Voltage	0.49*VddQ	0.50*VddQ	0.51*VddQ	V	5
VIH(DC)	High-Level Input Voltage	Vref + 0.18		VddQ+0.3	V	
VIL(DC)	Low-Level Input Voltage	-0.3		Vref - 0.18	V	
VIN(DC)	Input Voltage Level, CLK and /CLK	-0.3		VddQ + 0.3	V	
VID(DC)	Input Differential Voltage, CLK and /CLK	0.36		VddQ + 0.6	V	7
VTT	I/O Termination Voltage	Vref - 0.04		Vref + 0.04	V	6

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V $\pm$ 0.2V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Delta Cap.(Max.)	Unit	Notes
			Min.	Max.			
CI(A)	Input Capacitance, address pin	VI=1.25v f=100MHz VI=25mVrms	2.0	3.0	0.50	pF	11
CI(C)	Input Capacitance, control pin		2.0	3.0		pF	11
CI(K)	Input Capacitance, CLK pin		2.0	3.0	0.25	pF	11
CI/O	I/O Capacitance, I/O, DQS, DM pin		4.0	5.0	0.50	pF	11
CO(QF)	Output Capacitance, /QFC		2.0	3.0		pF	11

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V $\pm$ 0.2V, Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/Test Conditions	Organization	Limits(Max.)		Unit	Notes
			-75	-10		
IDD0	OPERATING CURRENT: One Bank; Active-Precharge; t RC = t RC MIN; t CK = t CK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	x4	105	95	mA	
		x8	110	105		
		x16	120	115		
IDD1	OPERATING CURRENT: One Bank; Active-Read-Precharge; Burst = 2; t RC = t RC MIN; CL = 2.5; t CK = t CK MIN; IOUT= 0mA; Address and control inputs changing once per clock cycle	x4	110	100		
		x8	115	110		
		x16	135	130		
IDD2P	PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; CKE $\leq$VIL (MAX); t CK = t CK MIN	x4/x8/x16	20	20		
IDD2N	IDLE STANDBY CURRENT: /CS $\geq$ VIH (MIN); All banks idle; CKE $\geq$ VIH (MIN); t CK = t CK MIN; Address and other control inputs changing once per clock cycle	x4/x8/x16	40	40		
IDD3P	ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; CKE $\leq$ VIL (MAX); t CK = t CK MIN	x4/x8/x16	40	40		
IDD3N	ACTIVE STANDBY CURRENT: /CS $\geq$ VIH (MIN); CKE $\geq$ VIH (MIN); One bank; Active-Precharge; t RC = t RAS MAX; t CK = t CK MIN; DQ,DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	x4	60	55		
		x8	65	60		
		x16	75	70		
IDD4R	OPERATING CURRENT: Burst = 2; Reads; Continuous burst;One bank active; Address and control inputs changing once per clock cycle;CL=2.5; t CK = t CK MIN; IOUT = 0 mA	x4	150	140		
		x8	170	160		
		x16	210	200		
IDD4W	OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL=2.5; t CK = t CK MIN;DQ, DM and DQS inputs changing twice per clock cycle	x4	145	135		
		x8	165	155		
		x16	200	180		
IDD5	AUTO REFRESH CURRENT: t RC = t RFC (MIN)	x4/x8/x16	190	180		
IDD6	SELF REFRESH CURRENT: CKE $\leq$ 0.2V	x4/x8/x16	3	3		9

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V $\pm$ 0.2V, Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter / Test Conditions	Limits		Unit	Notes
		Min.	Max.		
VIH(AC)	High-Level Input Voltage (AC)	Vref + 0.35		V	
VIL(AC)	Low-Level Input Voltage (AC)		Vref - 0.35	V	
VID(AC)	Input Differential Voltage, CLK and /CLK	0.7	VddQ + 0.6	V	7
VIX(AC)	Input Crossing Point Voltage, CLK and /CLK	0.5*VddQ - 0.2	0.5*VddQ + 0.2	V	8
IOZ	Off-state Output Current /Q floating Vo=0~VddQ	-5	5	μA	
II	Input Current / VIN=0 ~ VddQ	-2	2	μA	
IOH	Output High Current (VOUT = 1.95 V)	-16.8		mA	
IOL	Output High Current (VOUT = 0.35 V)	16.8		mA	

AC TIMING REQUIREMENTS

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V ±0.2V, Vss = VssQ = 0V, unless otherwise noted)

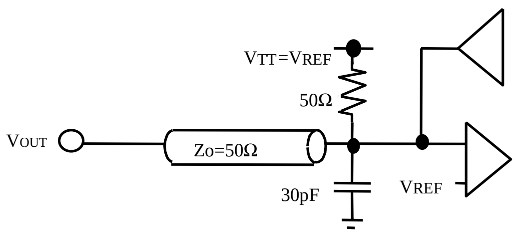
Symbol	AC Characteristics Parameter	-75		-10		Unit	Notes
		Min.	Max	Min.	Max		
tAC	DQ Output Valid data delay time from CLK//CLK	-0.75	0.75	-0.8	0.8	ns	
tDQSCK	DQ Output Valid data delay time from CLK//CLK	-0.75	0.75	-0.8	0.8	ns	
tCH	CLK High level width	0.45	0.55	0.45	0.55	ns	
tCL	CLK Low level width	0.45	0.55	0.45	0.55	ns	
tCK	CLK cycle time	7.5	15	8	15	ns	
		10	15	10	15	ns	
tDH	Input Setup time (DQ,DM)	0.5		0.6		ns	
tDS	Input Hold time(DQ,DM)	0.5		0.6		ns	
tDIPW	DQ and DM input pulse width (for each input)	1.75		2		ns	
tHZ	Data-out-high impedance time from CLK//CLK	-0.75	0.75	-0.8	0.8	ns	14
tLZ	Data-out-low impedance time from CLK//CLK	-0.75	0.75	-0.8	0.8	ns	14
tDQSQ	DQ Valid data delay time from DQS	-0.5	0.5	-0.6	0.6	ns	
tHP	Clock half period	tCLmin or tCHmin		tCLmin or tCHmin		ns	
tQH	Output DQS valid window	tHP-0.75		tHP-1.0		ns	
tDQSS	Write command to first DQS latching transition	0.75	1.25	0.75	1.25	tCK	
tDQSH	DQS input High level width	0.35		0.35		tCK	
tDQSL	DQS input Low level width	0.35		0.35		tCK	
tDSS	DQS falling edge to CLK setup time	0.2		0.2		tCK	
tDSH	DQS falling edge hold time from CLK	0.2		0.2		tCK	
tMRD	Mode Register Set command cycle time	15		15		ns	
tWPRES	Write preamble setup time	0		0		ns	16
tWPST	Write postamble	0.4	0.6	0.4	0.6	tCK	15
tWPRE	Write preamble	0.25		0.25		tCK	
tIS	Input Setup time (address and control)	0.9		1.2		ns	19
tIH	Input Hold time (address and control)	0.9		1.2		ns	19
tRPST	Read postamble	0.4	0.6	0.4	0.6	tCK	
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK	
tQPST	/QFC postamble during reads	0.4	0.6	0.4	0.6	tCK	
tQPRE	/QFC preamble during reads	0.9	1.1	0.9	1.1	tCK	
tQCK	/QFC output access time from CLK//CLK, for write		4		4	ns	
tQOH	/QFC output hold time for writes	1.25	2	1.25	2	ns	

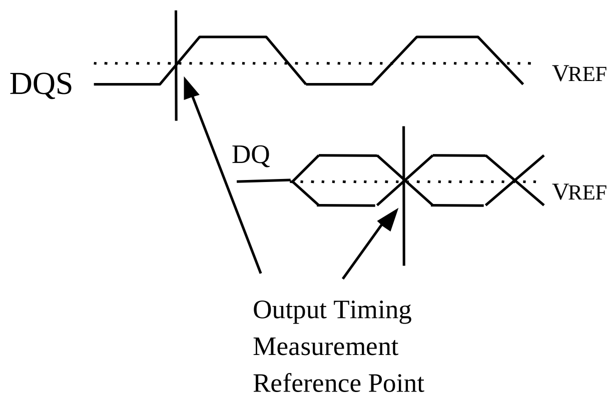
AC TIMING REQUIREMENTS(Continues)

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V $\pm$0.2V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	AC Characteristics Parameter	-75		-10		Unit	Notes
		Min.	Max	Min.	Max		
tRAS	Row Active time	45	120,000	50	120,000	ns	
tRC	Row Cycle time(operation)	65		70		ns	
tRFC	Auto Ref. to Active/Auto Ref. command period	75		80		ns	
tRCD	Row to Column Delay	20		20		ns	
tRP	Row Precharge time	20		20		ns	
tRRD	Act to Act Delay time	15		15		ns	
tWR	Write Recovery time	15		15		ns	
tDAL	Auto Precharge write recovery + precharge time	35		35		ns	
tWTR	Internal Write to Read Command Delay	1		1		tCK	
tXSNR	Exit Self Ref. to non-Read command	75		80		ns	
tXSRD	Exit Self Ref. to -Read command	200		200		tCK	
tXPNR	Exit Power down to command	1		1		tCK	
tXPRD	Exit Power down to -Read command	1		1		tCK	18
tREFI	Average Periodic Refresh interval	15.6		15.6		μs	17

Output Load Condition

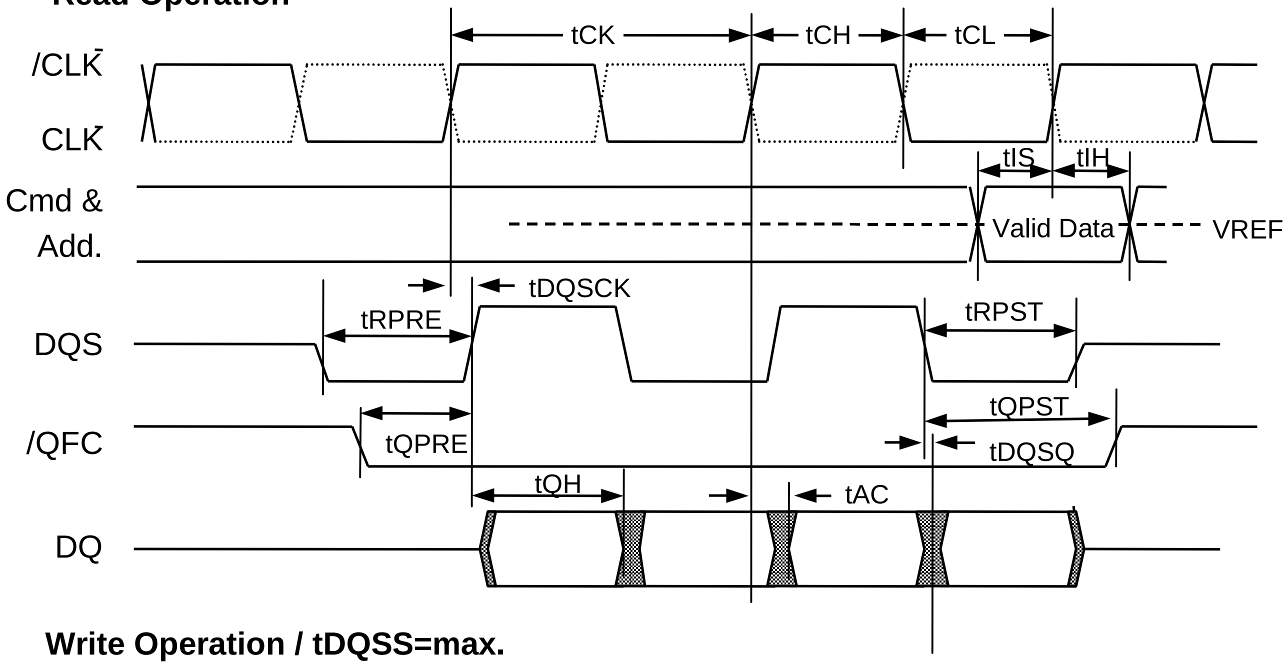




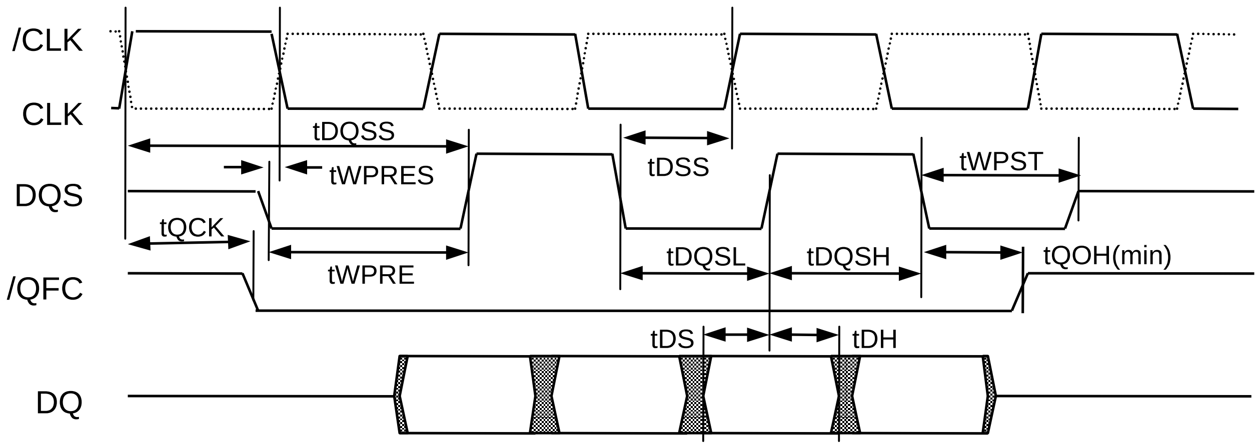
Notes

1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*VddQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed $\pm$2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*VddQ of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized.
11. This parameter is sampled. VddQ = 2.5V$\pm$0.2V, Vdd = 2.5V $\pm$ 0.2V , f = 100 MHz, Ta = 25°C, VOUT(DC) = VddQ/2, VOUT(PEAK TO PEAK) = 25mV. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
12. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE$\leq$ 0.3VddQ is recognized as LOW.
14. t HZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
17. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
18. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the power down mode.
19. For command/address and CK & /CK slew rate > 1.0V/ns.

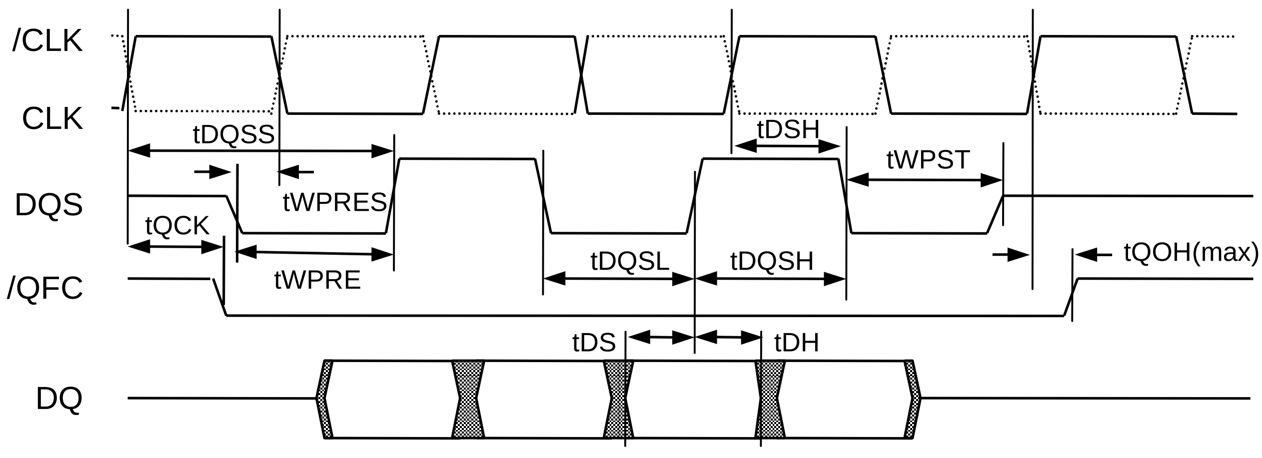
Read Operation



Write Operation / tDQSS=max.



Write Operation / tDQSS=min.



OPERATIONAL DESCRIPTION

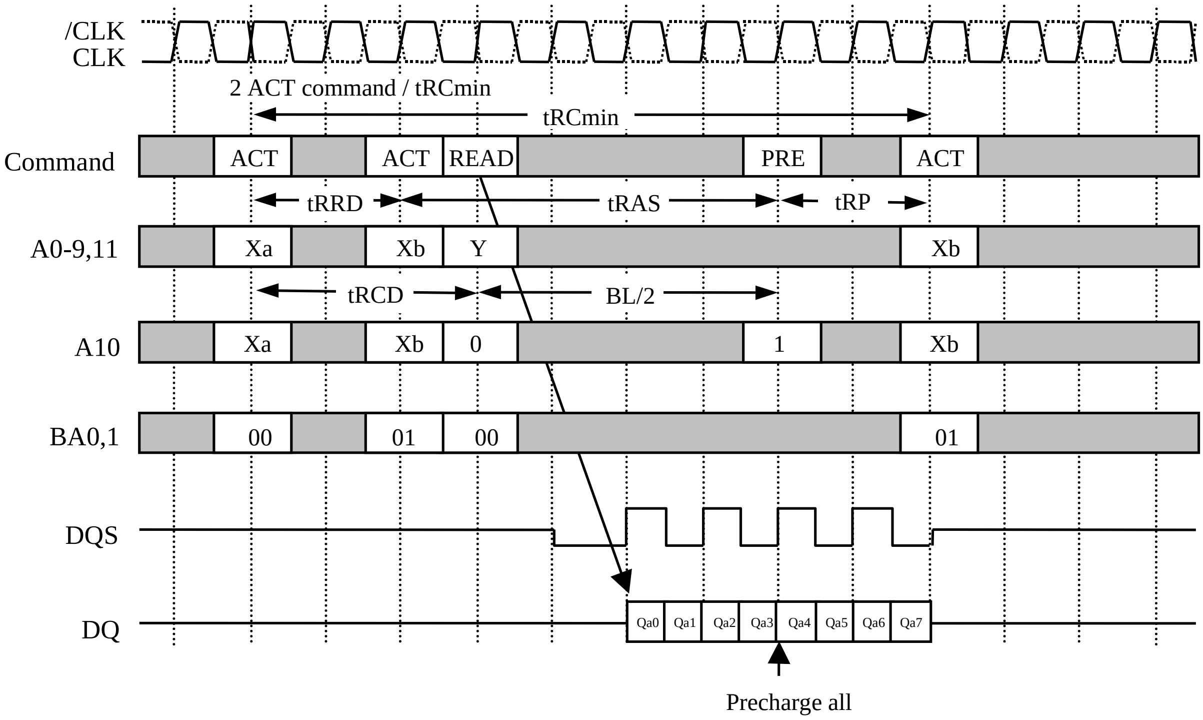
BANK ACTIVATE

The DDR SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row address A11-0. The minimum activation interval between one bank and the other bank is tRRD. Maximum 2 ACT commands are allowed within tRC,although the number of banks which are active concurrently is not limited.

PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA,PRE+A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.

Bank Activation and Precharge All (BL=8, CL=2)

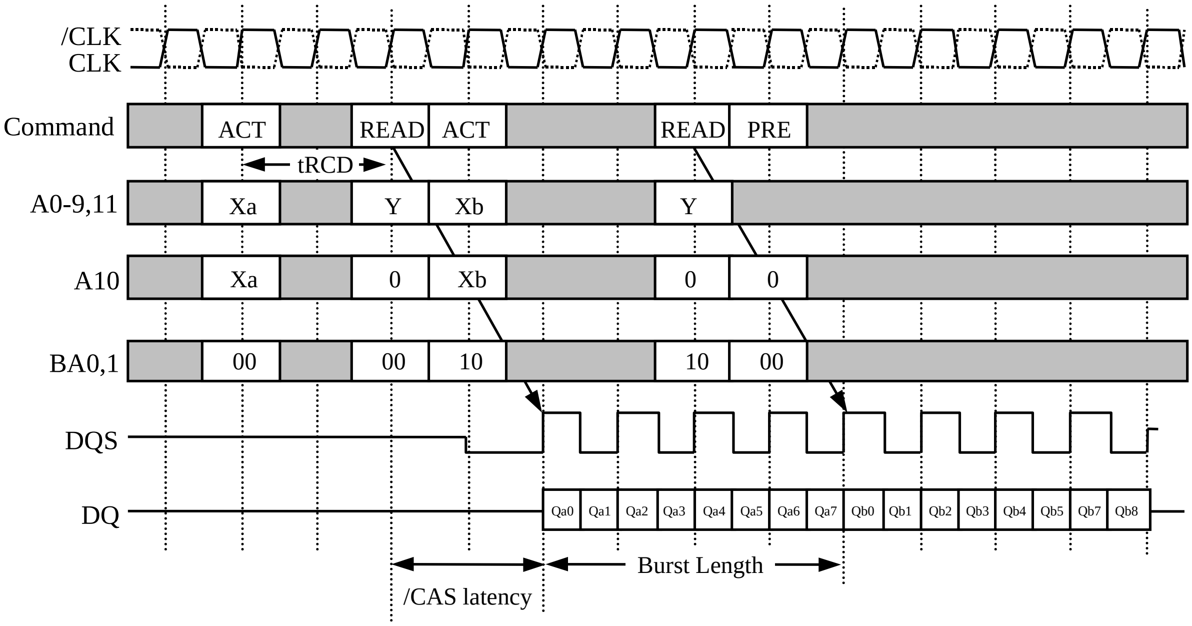


A precharge command can be issued at BL/2 from a read command without data loss.

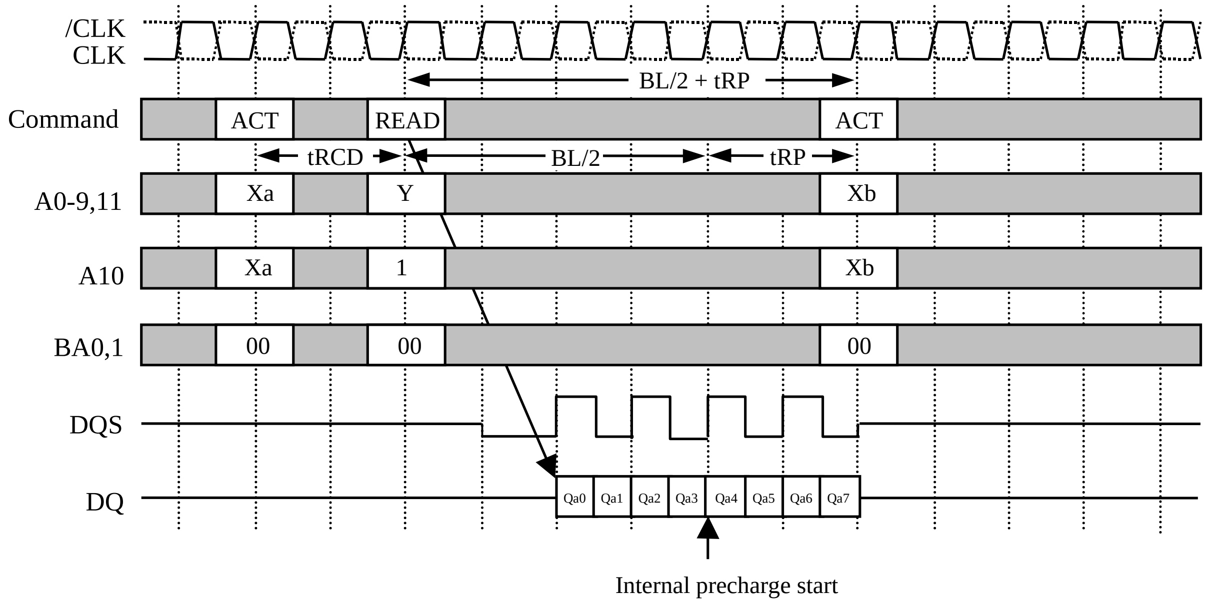
READ

After tRCD from the bank activation, a READ command can be issued. 1st Output data is available after the /CAS Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by A11,A9-A0(x4)/A9-A0(x8)/A8-A0(x16), and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is high at a READ command, the auto-precharge (READA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL/2 after READA. The next ACT command can be issued after (BL/2+tRP) from the previous READA.

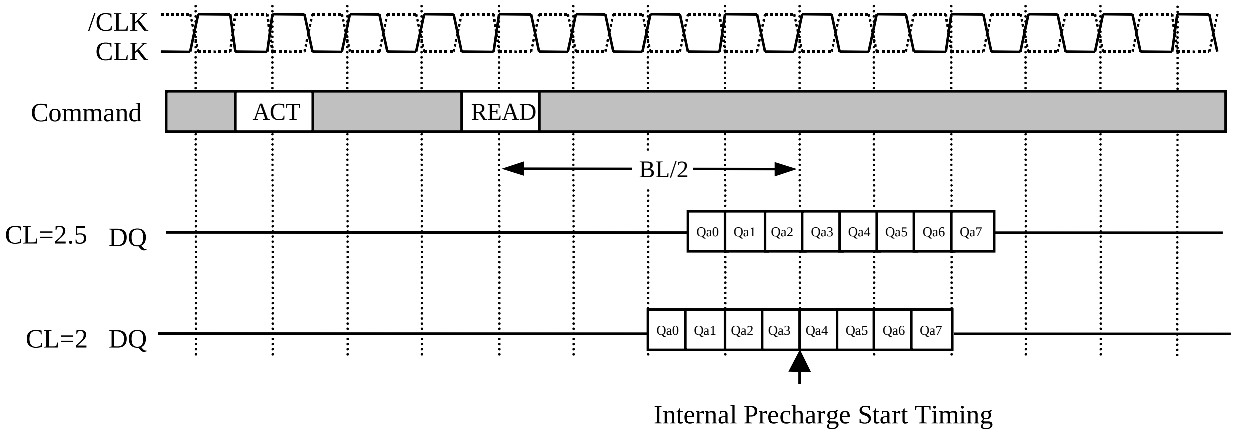
Multi Bank Interleaving READ (BL=8, CL=2)



READ with Auto-Precharge (BL=8, CL=2)



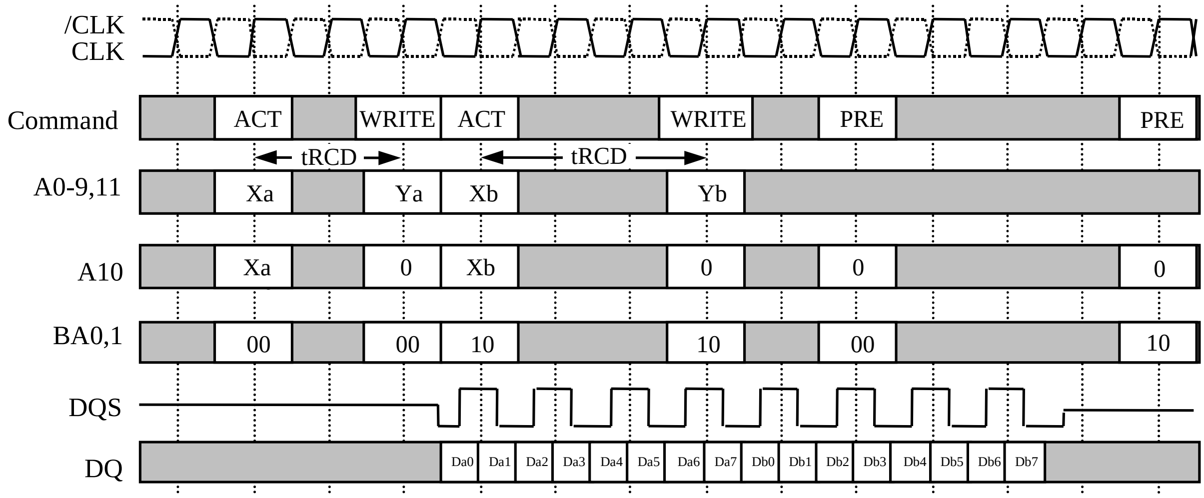
READ Auto-Precharge Timing (BL=8)



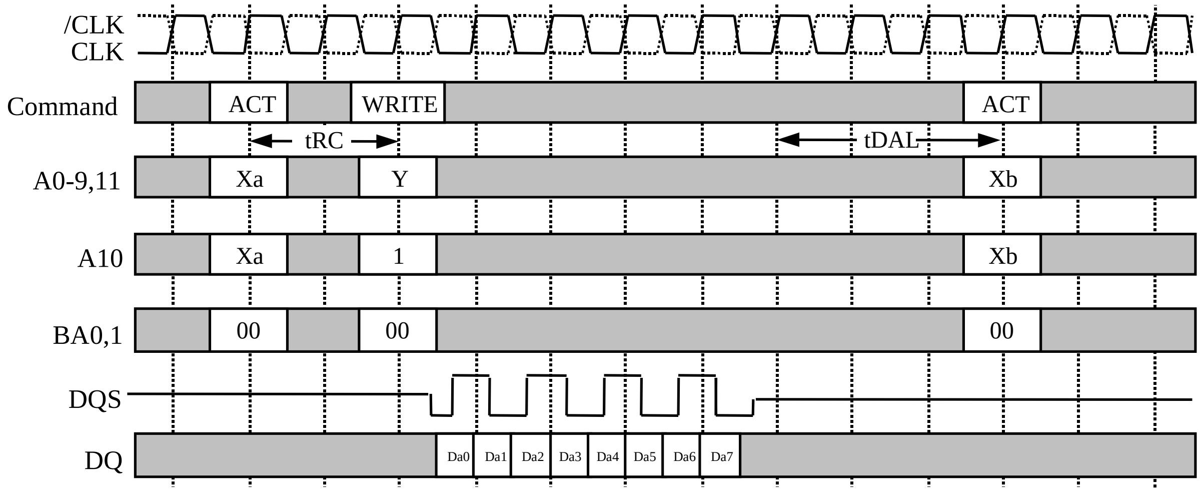
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set from the WRITE command with data strobe input, following (BL-1) data are written into RAM, when the Burst Length is BL. The start address is specified by A11,A9-A0(x4)/A9-A0(x8)/A8-A0(x16), and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last data to the PRE command, the write recovery time (tWRP) is required. When A10 is high at a WRITE command, the auto-precharge(WRITEA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The next ACT command can be issued after tDAL from the last input data cycle.

Multi Bank Interleaving WRITE (BL=8)



WRITE with Auto-Precharge (BL=8)

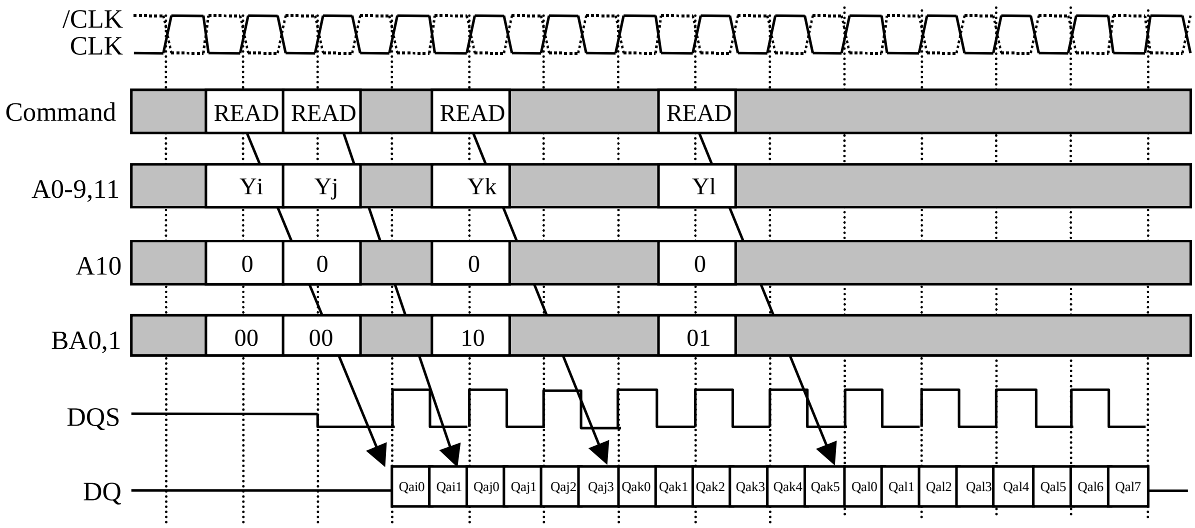


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1CLK.

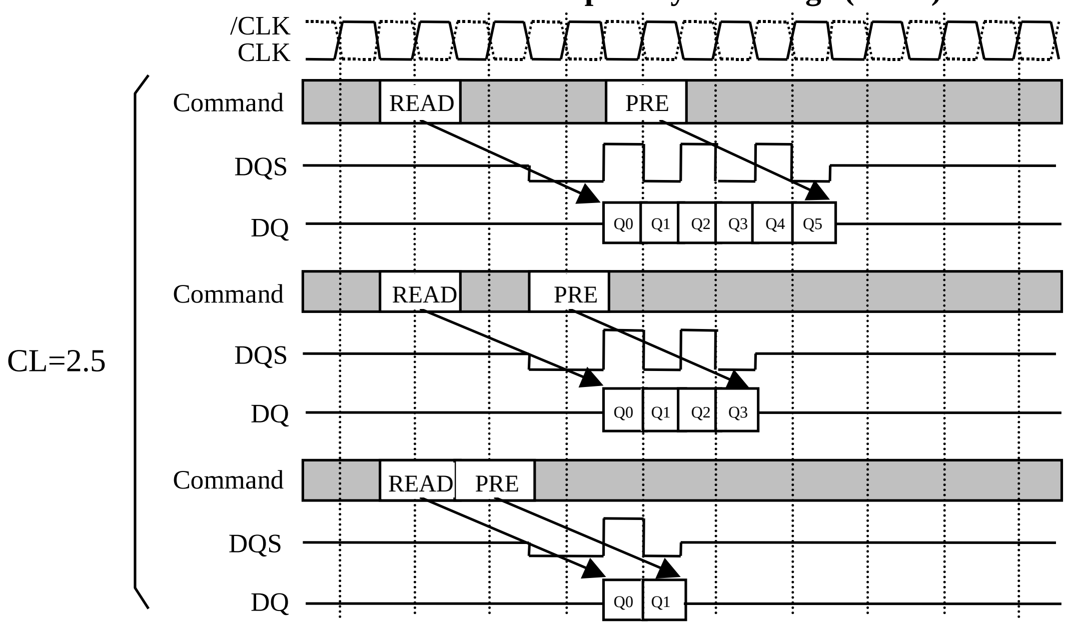
Read Interrupted by Read (BL=8, CL=2)



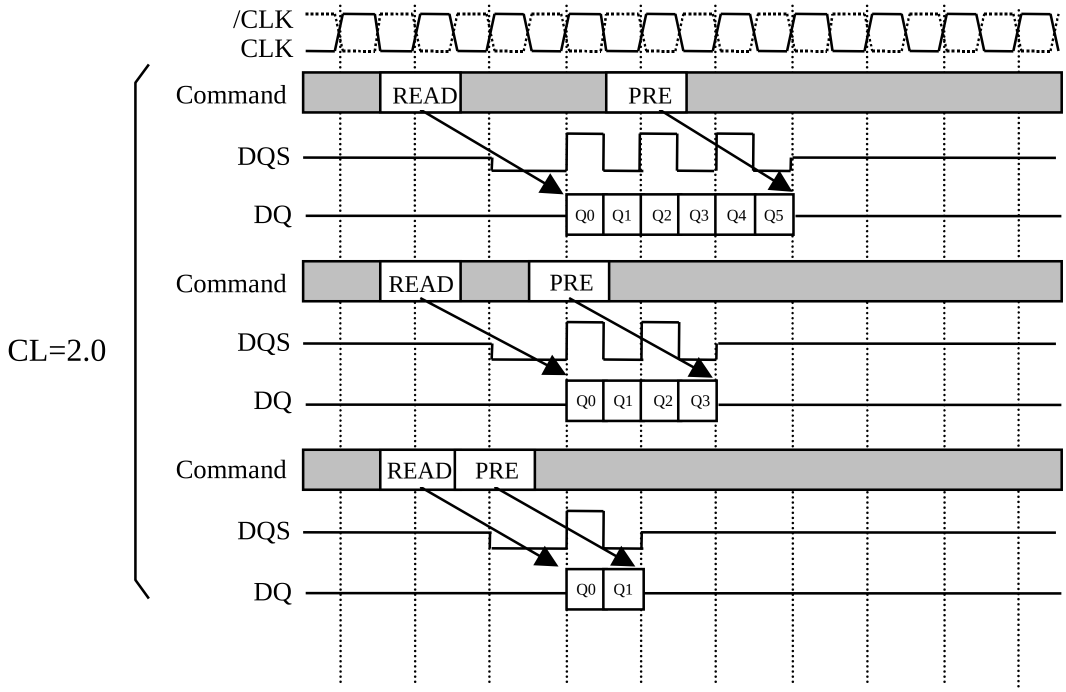
[Read Interrupted by precharge]

Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=8.

Read Interrupted by Precharge (BL=8)



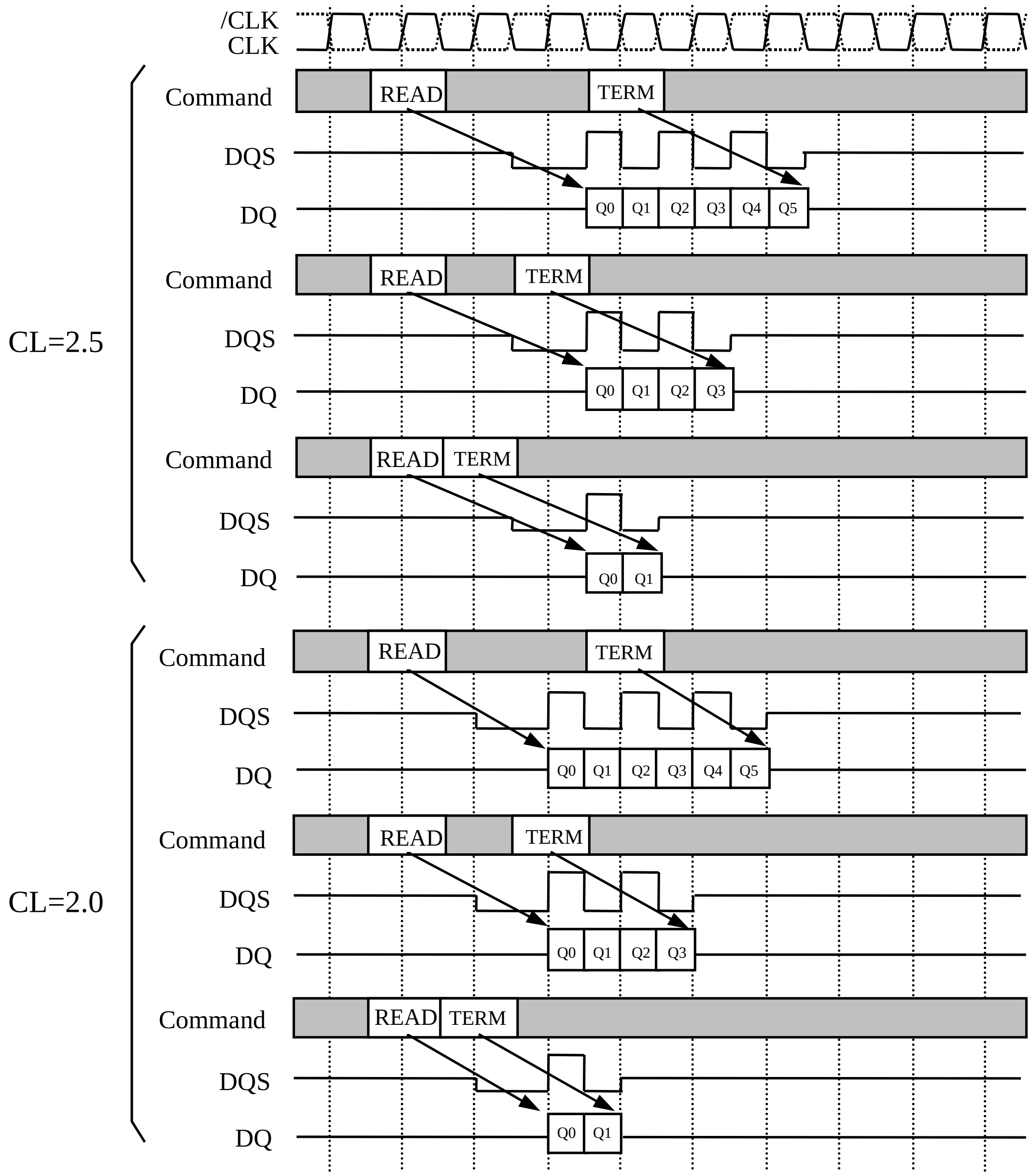
Read Interrupted by Precharge (BL=8)



[Read Interrupted by Burst Stop]

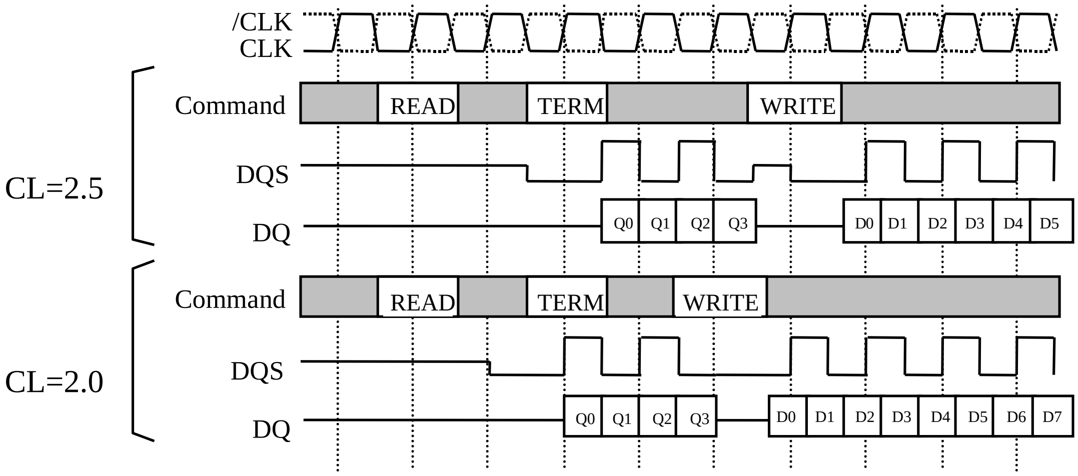
Burst read operation can be interrupted by a burst stop command(TERM). READ to TERM interval is minimum 1 CLK. A TERM command to output disable latency is equivalent to the /CAS Latency. As a result, READ to TERM interval determines valid data length to be output. The figure below shows examples of BL=8.

Read Interrupted by TERM (BL=8)



[Read Interrupted by Write with TERM]

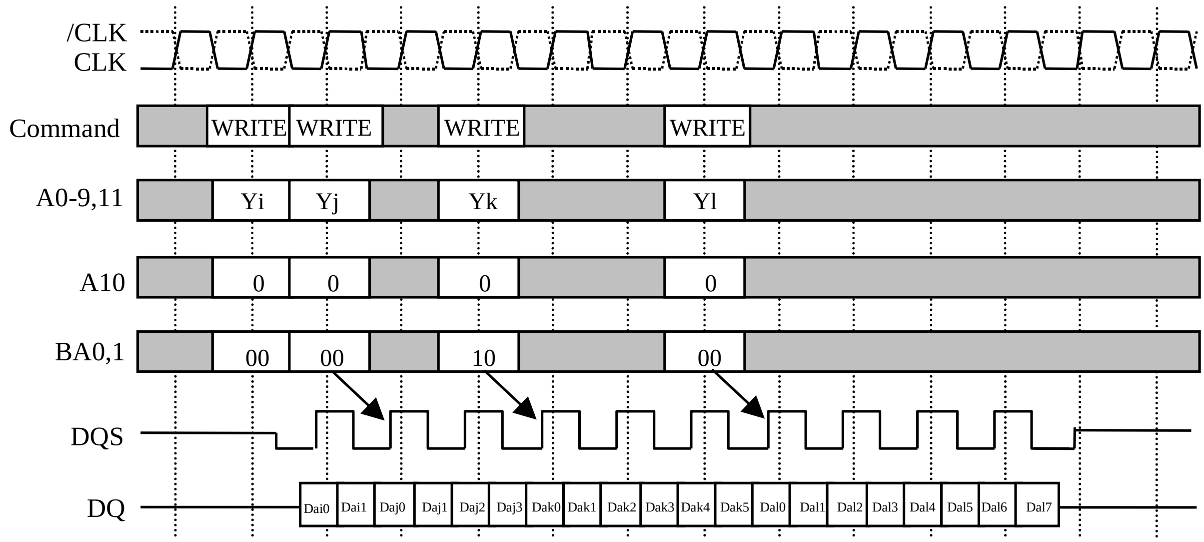
Read Interrupted by TERM (BL=8)



[Write interrupted by Write]

Burst write operation can be interrupted by write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

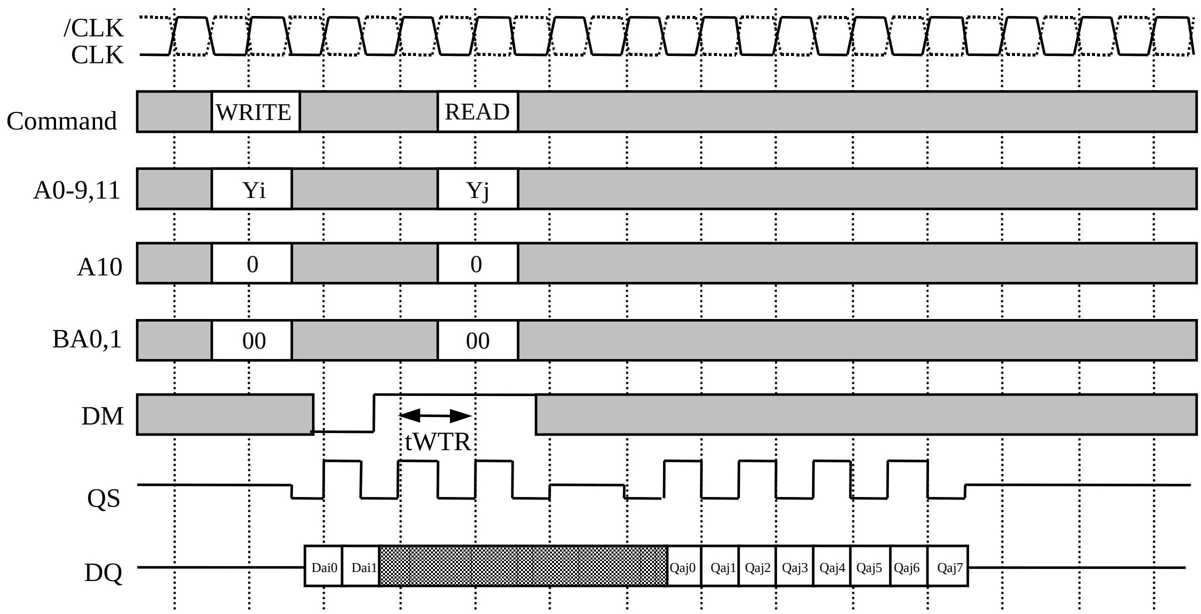
Write Interrupted by Write (BL=8)



[Write interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. Internal WRITE to READ command interval(tWTR) is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care". tWTR is referenced from the first positive edge after the last data input.

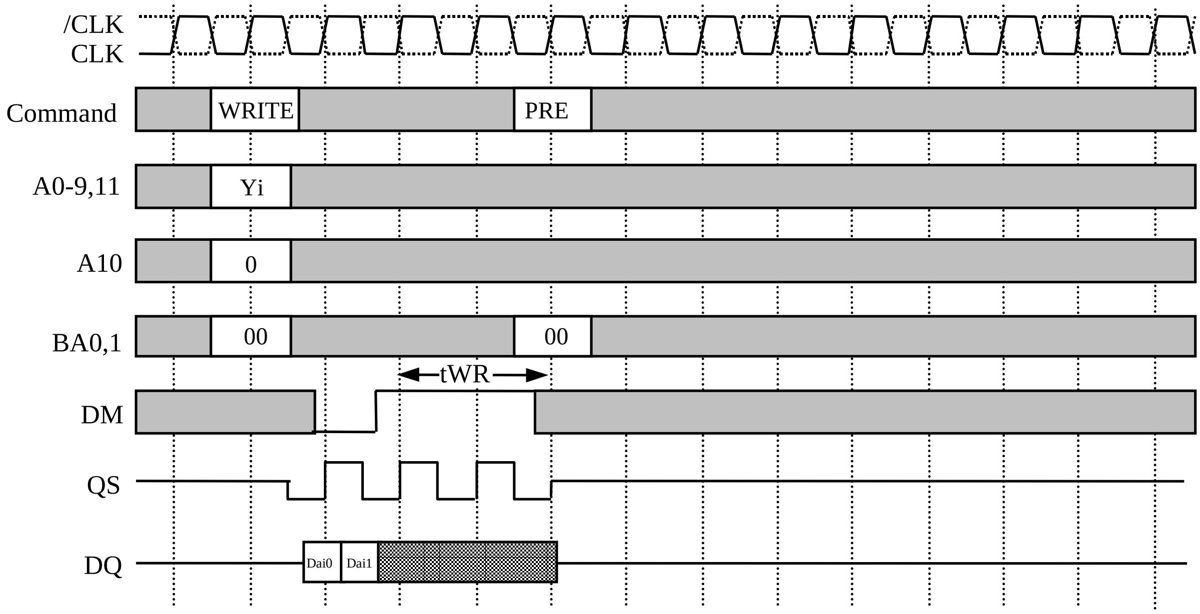
Write Interrupted by Read (BL=8, CL=2.5)



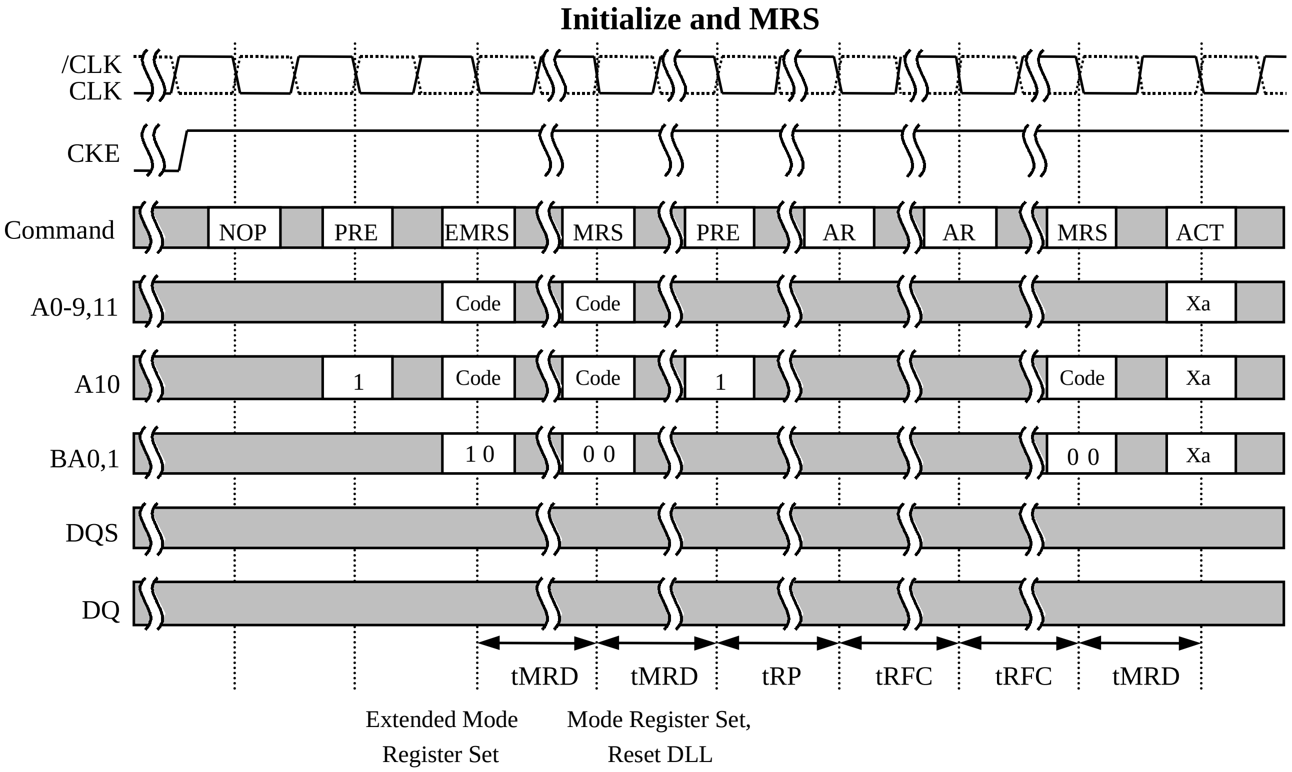
[Write interrupted by Precharge]

Burst write operation can be interrupted by precharge of the same or all bank. Random column access is allowed. tWR is referenced from the first positive CLK edge after the last data input.

Write Interrupted by Precharge (BL=8, CL=2.5)

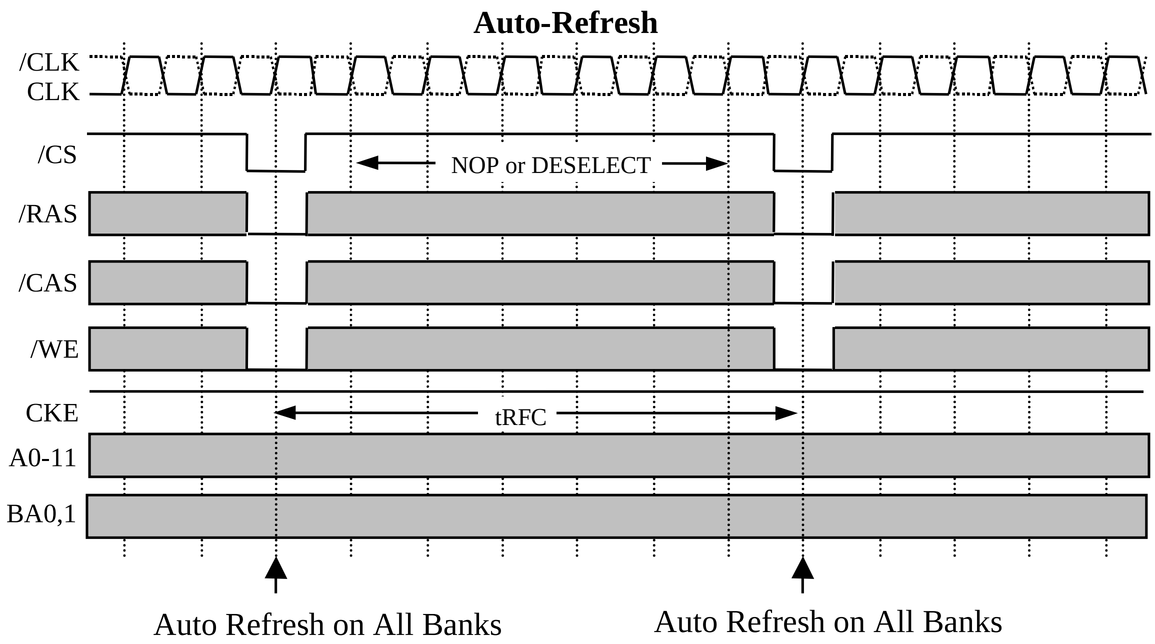


[Initialize and Mode Register sets]



[AUTO REFRESH]

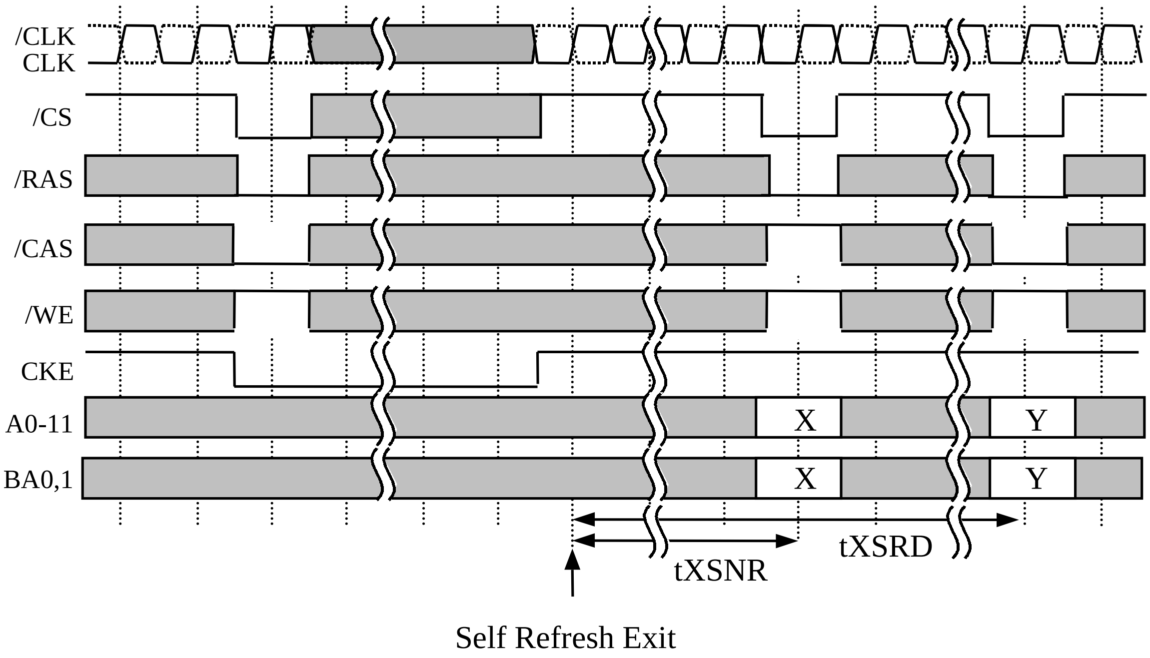
Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L,/WE=CKE=H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 128Mbits memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRFC . Any command must not be supplied to the device before tRFC from the REFA command.



[SELF REFRESH]

Self -refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L,/WE=H,CKE=L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enable input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR/tXSRD.

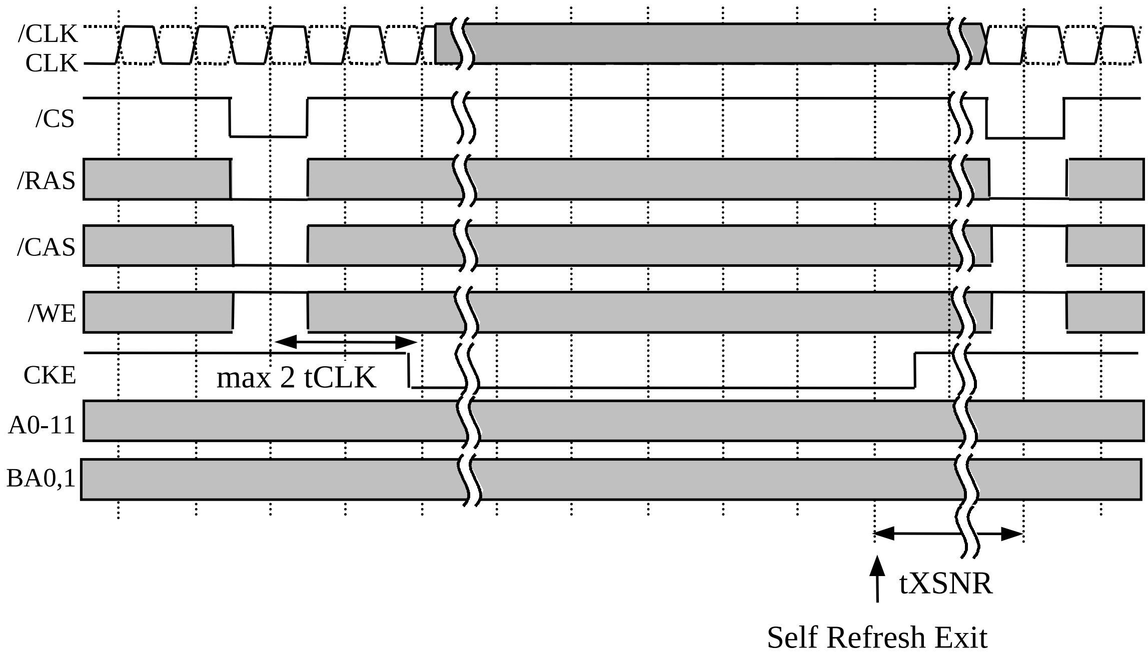
Self-Refresh



[Asynchronous SELF REFRESH]

Asynchronous Self -refresh mode is entered by CKE=L within 2 tCLK after issuing a REFA command (/CS=/RAS=/CAS=L,/WE=H). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enable input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR/tXSRD.

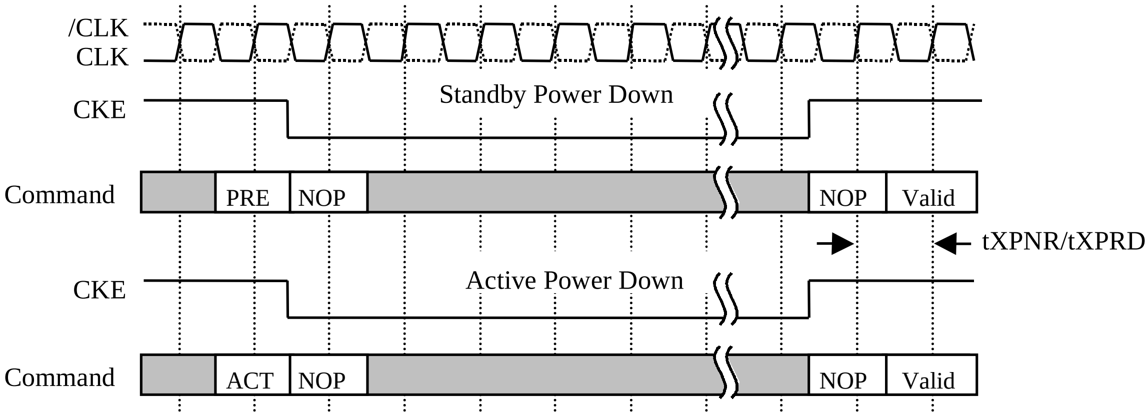
Asynchronous Self-Refresh



[Power DOWN]

The purpose of CLK suspend is power down. CKE is synchronous input except during the self-refresh mode. A command at cycle is ignored. From CKE=H to normal function, DLL recovery time is NOT required in the condition of the stable CLK operation during the power down mode.

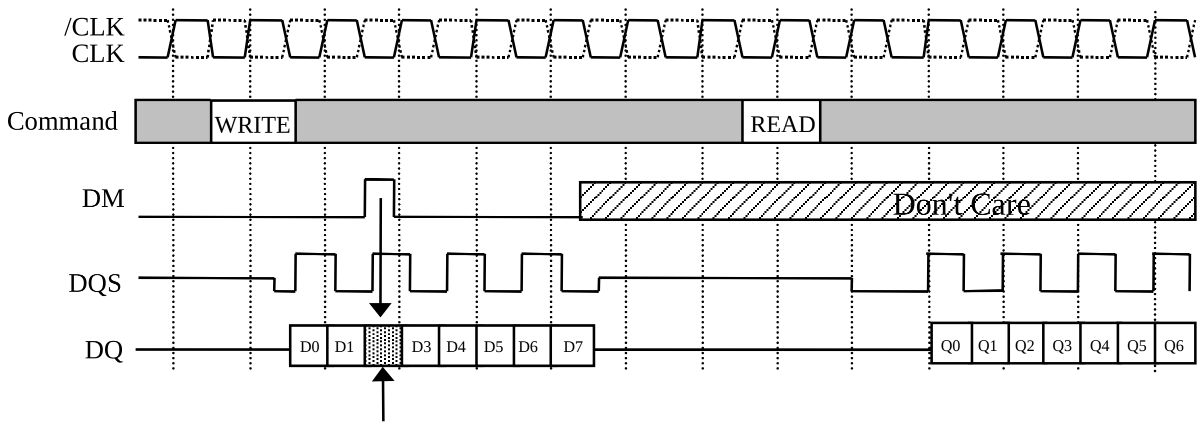
Power Down by CKE



[DM CONTROL]

DM is defined as the data mask for writes. During writes,DM masks input data word by word. DM to write mask latency is 0.

DM Function(BL=8,CL=2)



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